Characterization of Si *pn* junctions fabricated by direct wafer bonding in ultra-high vacuum

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The electrical characteristics of *pn* junctions formed by direct bonding of silicon wafers in ultra-high vacuum have been quantified. The bonding process produces low reverse leakage <1 μA/cm^2 and near-ideal forward current. The observation of bulk-like bonded interfaces is supported by transmission electron microscopy and infra-red transmission imaging. © *1998 American Institute of Physics.* [S0003-6951(98)02409-7]

Direct bonding of semiconductor materials, mainly (100) Si wafers, has been studied by several groups.[1,2] The impact that direct wafer bonding will have on the semiconductor industry, however, depends on the electrical properties of the interface, which is an area that has had only limited attention.[3–5] To date, direct wafer bonding has encompassed many pre- and post-bonding processing techniques. Hydrophobic bonding is preferred over hydrophilic bonding for low temperature processing, since the latter requires high temperatures to dissolve the interfacial oxide into the bulk Si and to reduce the associated electronic barrier. Hydrophobic bonding, however, is susceptible to void formation through creation of gas bubbles thought to be hydrogen diffusing to hydrocarbon contamination sites and subsequent formation of methane.[6] A recently demonstrated bonding technique that removes hydrogen from the hydrophobic surface utilizes ultra-high vacuum (UHV) annealing prior to bonding.[7] In that work, bonding was also performed in UHV near room temperature. In this work, a similar process is used to fabricate *pn* junctions where the metallurgical junction and the bonded interface are coincident. The electrical properties of the junctions are characterized.

The goal of this work is to reduce process temperatures both prior to and following wafer bonding, since an important application of low temperature wafer bonding is the fabrication of double-sided power devices.[8] If process temperatures are maintained below 450 °C (sintering temperature of Al:Si contacts), fully processed devices could be bonded after appropriate back side processing (e.g., lapping and polishing). The use of barrier metals would increase the safe temperature to 500–550 °C. This certainly precludes hydrophilic bonding which requires anneal temperatures $\geqslant$1200 °C.[4] Hydrophobic bonding also requires anneal temperatures in excess of 600 °C to allow the H to diffuse away from the interface and complete the bonding[2] although incomplete removal of H apparently does not preclude device quality interface formation.[9]

From the standpoint of creating ideal bonded interfaces using low temperature processes, the UHV bonding process is very attractive. Adsorbed gases (hydrogen in the case of hydrophobic surfaces) and contaminants can be largely removed from the surface prior to bonding. Once this atomically clean surface is prepared, the driving force for bonding is large since the surface energy of unpassivated Si is very high [1.36 J/m^2 (Ref. 10)]. On the (001) Si surface, the slight reduction in surface energy produced by the (2×1) reconstruction appears to not impede the bonding process and the reconstruction is readily broken. This may not be true for (111) surfaces which undergo more complicated reconstruction [e.g., (7×7)]. In this work, UHV bonding has been investigated and *pn* diodes have been fabricated and characterized. Physical characterization techniques, including cross-sectional transmission electron microscopy (TEM), crack propagation measurements, and infra-red (IR) imaging, were also performed.

Several 75 mm Si wafer types were used for the bonding experiments. For *pn* junction fabrication, n^+ substrates with n-epitaxial layers (4.5 μm, 1.5×10^{15} cm^{-3}) were bonded to p^+ (0.01 Ω cm) substrates. Alternately, p$^-$ substrates (10 Ω cm) were bonded for process characterization. The following hydrophobic cleaning procedure was used: nitric acid boil and de-ionized water (DI) rinse followed by a standard SC-1 and DI rinse followed by a 30 s 10:1 DI:HF dip. The HF-last process was always performed without a DI rinse following the HF dip. The wafers were mounted in a specially designed Ta substrate holder and wafer separation was maintained by a single 0.125-mm-thick Ta clip that could be manipulated from outside the UHV chamber. Following cleaning and mounting the wafers were immediately introduced into the UHV chamber via a cryo-pumped fast entry loadlock. The base pressure of the cyro- and ion-pumped chamber was 10^{-10} Torr or better. After mounting in a Ta heater assembly the separated wafer pair was baked for 1 hr at 200 °C. After baking the wafer temperature was ramped quickly to $\sim$550 °C at which point a sharp pressure increase (up to 2×10^{-8} Torr), representing the desorbing hydrogen, was observed.[11] Heating was ceased and the wafers were bonded at various temperatures following the hydrogen desorption step by removing the Ta clip separating the wafers as the target temperature was reached. The bonding process

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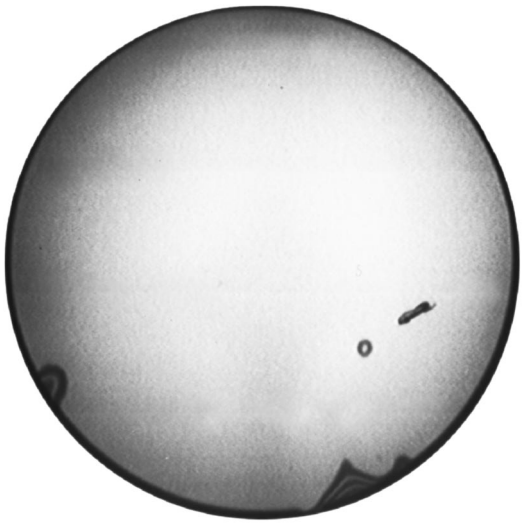

FIG. 1. Infrared transmission image of 75 mm wafer pair bonded in UHV.

was observed in one case with an IR transmission imaging setup. Once the Ta clip was removed, wafer bonding was immediate and spontaneous. In no case was external pressure applied to the wafer pair to initiate bonding.

Devices were prepared using a special mesa fabrication process. First Pt:Au metallization was deposited on both surfaces. The wafers were quartered and the diodes were isolated by forming deep ($\sim$450 μm) trenches on a regular grid. The trenches were produced with a 0.002 in. diamond saw. Following a partial sawing process the wafers were etched in a solution of 3:5:3 HF:HNO_3:CH_3COOH (Si etch rate approximately 80 μm/min) for 30 s followed by a DI rinse to remove damage produced by the sawing process. The Au metallization was unaffected by the etching step. Alternatively, Al was deposited after sawing and etching by using an angled evaporation process which effectively shadowed the junction area due to the high aspect ratio of the trench.

The bonding process was characterized by IR imaging, TEM, and crack propagation measurements following removal from the UHV chamber. IR imaging was performed with a charge coupled device (CCD) camera and tungsten-halogen lamp. IR imaging of the as-bonded wafers often showed no voids but typically a few were observed (see Fig. 1). The voids that were observed were presumably due to particulates and not gas bubbles as no hydrogen remained on the surface during bonding. The low number of observable voids was surprising since the cleaning and loading of the substrates were not performed under clean room conditions. Crack propagation measurements[12] were performed to characterize the interface energy. Wafer delamination was not possible and only three-dimensional fracture occurred at the wafer edge. Although inconclusive, the results indicate a very high bond strength was achieved by this bonding technique. The quality of the bonded interface was further studied by high-resolution cross-sectional TEM. Figure 2(a) is a TEM micrograph showing the interface region of a wafer pair that was bonded at approximately 350 °C after desorbing H at $\sim$550 °C. The interface is smooth and the respective lattices appear to be in registry. The quality of the interface appears to be a strong function of wafer cleaning. Figure

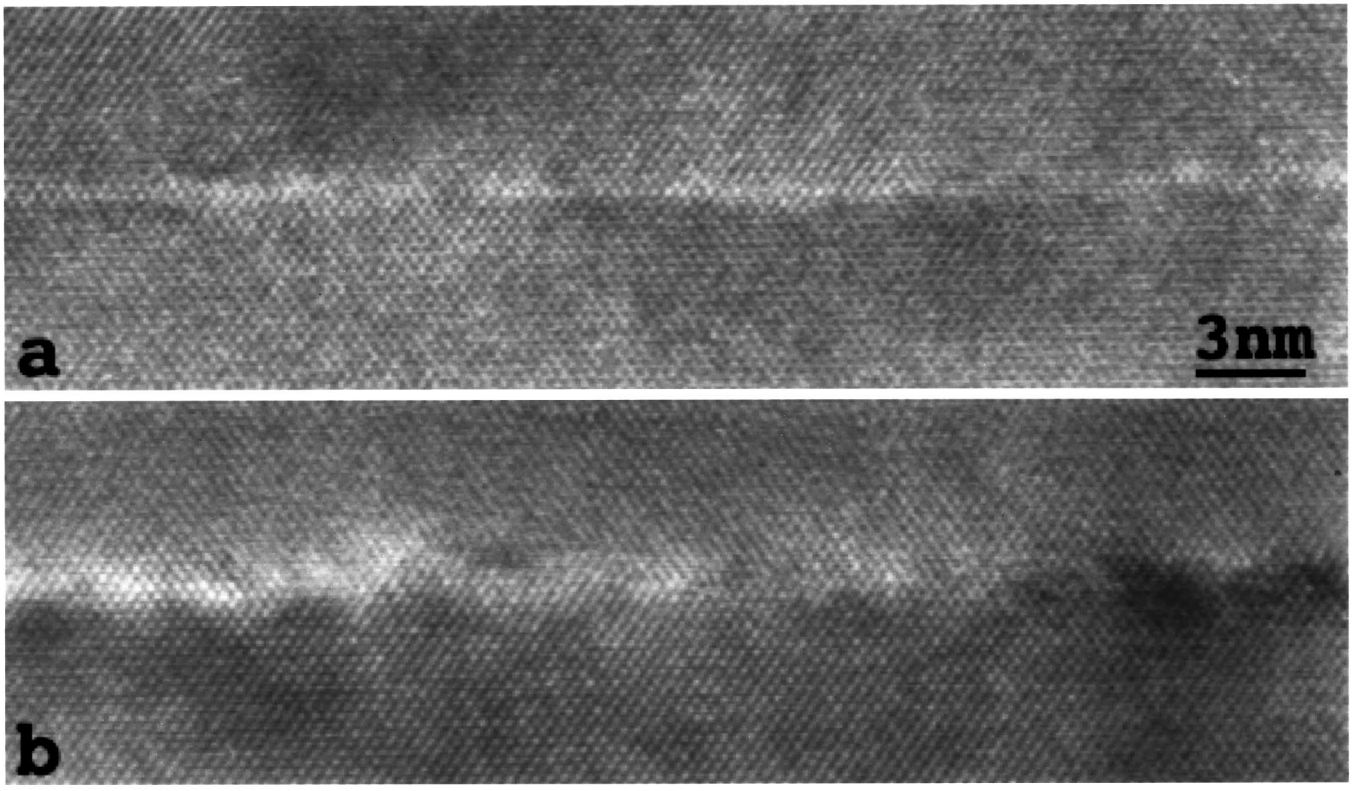

FIG. 2. High resolution cross-sectional transmission electron micrograph of (a) a ''clean'' bonded interface and (b) a carbon contaminated bonded interface.

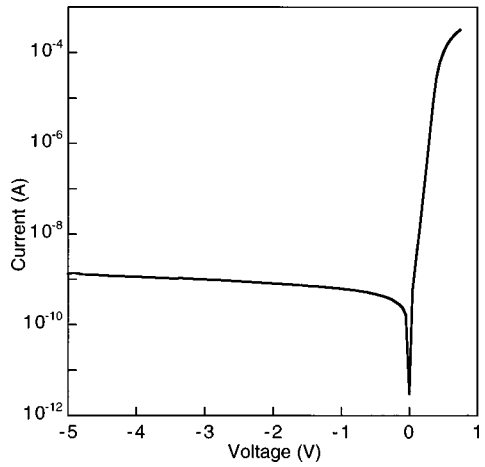

FIG. 3. Current-voltage characteristics of a *pn* junction fabricated by UHV direct wafer bonding.

2(a) is contrasted with the micrograph of Fig. 2(b) where a known carbon contamination coverage ($\sim$5% of a monolayer as determined by x-ray photoelectron spectroscopy) was present on each surface prior to bonding using otherwise similar conditions as above. The respective lattices are in registry but the bonded interface appears rough. The effect on interface roughness is substantial, illustrating the importance of surface preparation as well as vacuum chamber cleanliness. The slight contrast feature observed at the ''clean'' interface of Fig. 2(a) is not understood but is possibly due to strain at the interface. This interpretation would be consistent with molecular dynamics simulations of low temperature bonding of (2×1) reconstructed Si(100) surfaces.[13] The simulations also showed that this interface relaxes into a network of screw dislocations upon high temperature annealing, consistent with TEM observations of hydrophobic bonding and high temperature annealing.[14]

The *pn* junctions were bonded and diodes were fabricated as described above. The bonding temperature was $\sim$400 °C. Current-voltage characterization was performed on a HP4145 parameter analyzer and the results are shown in Fig. 3 for a 1×1 mm^2 diode. The diodes exhibited low reverse leakage and near-ideal forward characteristics. The reverse leakage current density of ~0.1 μA/cm^2 for this device is believed to be the lowest achieved for low temperature directly bonded *pn* junctions.[15] Since the bonding was performed at low temperature with no subsequent annealing step, no diffusion is expected; it is believed that the bonded junction is abrupt and coincident with the metallurgical junction. The ideality of the forward current was determined by a least squares fit to $I=I_0e^{qV/nkT}$. The least squares fit yielded an ideality factor, n, of 1.18. This represents the lowest reported ideality for low temperature bonded junctions and is indicative of low recombination at the bonded interface.

Summarizing, it has been demonstrated that low temperature bonding under UHV conditions produces a near-ideal, bulk-like interface. Through TEM characterization, it has been shown that surface preparation must be performed carefully to prevent interface roughness. Electrical characterization of *pn* junctions formed by UHV bonding at low temperature indicates low defect density at the bonded interface.

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